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# Elimination of Charge Sharing Problem in Dynamic Circuits

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***Abstract*** **- A technology is proposed in this literature to significantly reduce the charge sharing problem in the dynamic circuits due to the generation of the parasitic capacitor at each node. Here we used a weak PMOS pull-up device (with a small W/L ratio) to the dynamic CMOS stage output to reduce the influence of the parasitic capacitor.**

***Keywords*** **- CMOS, Domino Logic, NMOS, PMOS, Weaker PMOS.**

## I. INTRODUCTION

The digital integrated circuit charge sharing problem has become one of the foremost issues in the design of very deep submicron VLSI chips. Charge sharing in digital circuits refers to any phenomenon that causes the voltage at a node to diverge from its nominal value. While these charge sharing always existed in the past they had little effect on the performance of integrated circuits and were often ignored. It is the unstopped aggressive technology scaling in an effort to constantly improve chip performance and integration level that makes charge sharing plays a gradually significant role in comparison with conventional design metrics like area, speed and power consumption.

Together with technology scaling, aggressive design practices like using dynamic logic styles have also seen broader use in recent years to attain higher performance of integrated circuits. Circuits design using dynamic logic style can be significantly faster and more compact then their static CMOS technique. This is specifically the case with wide fan-in dynamic logic gates where a single gate can realize the logic function that otherwise would involve multiple levels of static CMOS logic gates. Therefore, wide fan-in dynamic gates are regularly employed in performance-critical blocks of high performance chips, such as in microprocessor, digital signal processor, and so on.

In this paper, we propose a novel design method to improve the charge sharing problem tolerance of dynamic circuits by studies their results by simulation. We will show that dynamic logic gates are not essentially less charge sharing problem tolerant if proper charge sharing problem tolerant design techniques are employed. In fact, using the proposed method in this paper, charge sharing tolerance of dynamic logic circuits can be improved beyond the level of static CMOS logic gates while still hold their advantage in performance. The proposed charge sharing tolerant design method can be grasped using a number of different circuits and therefore having broader effect.

## II. DYNAMIC CIRCUIT

In the dynamic CMOS circuit technique, clock pulse is given between a PMOS and a NMOS and the NMOS logic is associated between them. The circuit operation is based on first precharging the output node capacitance and subsequently estimating the output level according to the applied inputs. Together these operations are scheduled by a single clock signal which drives one NMOS and one PMOS transistors in each dynamic stage.

When the clock signal is high then precharge transistor p1 turns off and n1 turns on. If the input signal forms a conducting path between the output node and ground then output capacitance will discharge to 0V.When the clock signal is low the PMOS transistor p1 is conducting and the complementary NMOS transistor n1 is off .The output capacitance of the circuit is charged up through the conducting PMOS transistor to a logic high level of VDD.

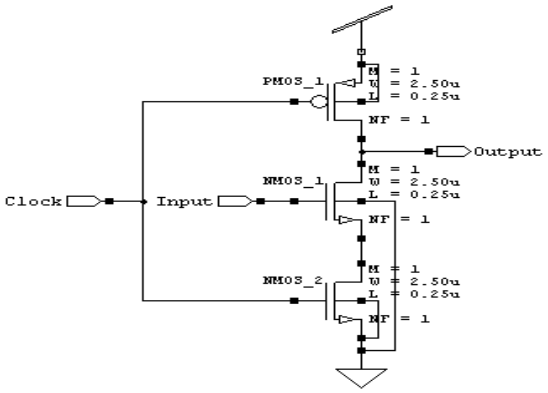


Fig.1. CMOS Dynamic inverter

Above we have implemented the dynamic inverter by using simulation and generated its waveform. Fig,2 shows that there is a problem in dynamic circuit, in the evaluation phase if the input is low the capacitance is already charge to VDD but due to the charge sharing at each node of NMOS logic, it will be corrupted.

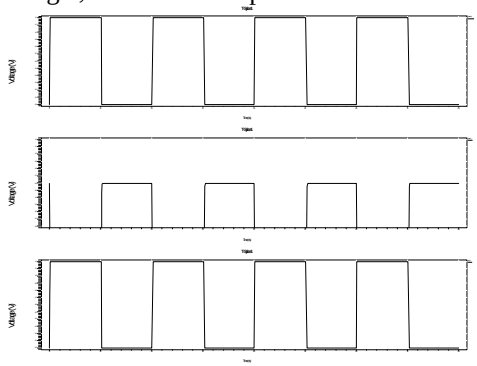

Fig.2.Waveform for CMOS dynamic inverter

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## III. Domino Logic

In the domino logic, we associated a static CMOS inverter at the output of the dynamic circuit. During the precharge phase (when clock is 0), the output node of the dynamic CMOS stage is precharged to high logic level, and the output of the CMOS inverter becomes low. When the clock signal rises at the starting of the evaluation phase, there are two possibilities: The output node of the dynamic CMOS stage is either discharged to 0v through the NMOS circuitary (1 to 0 transition), or it remains high. Consequently, the inverter output voltage can also make at most one transition during the evaluation phase, from 0 to1.Regardless of the input voltage applied to the dynamic CMOS stage, it is not probable for the CMOS inverter to make a 1 to 0 transition during the evaluation phase.

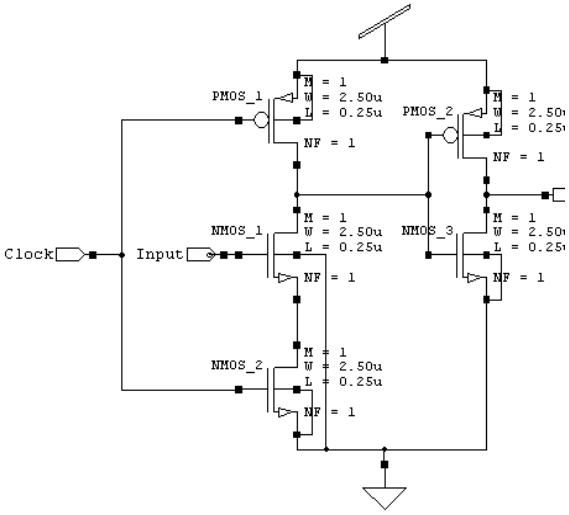


Fig.3. Domino logic

Above we have implemented the domino logic by using simulation and generated its waveform. Fig.4 shows that there are some restrictions in the domino logic. First, only non-inverting structure can be realized and second charge sharing between the dynamic stage output node and the intermediate nodes of the NMOS logic block during the evaluation phase may cause inaccurate outputs.

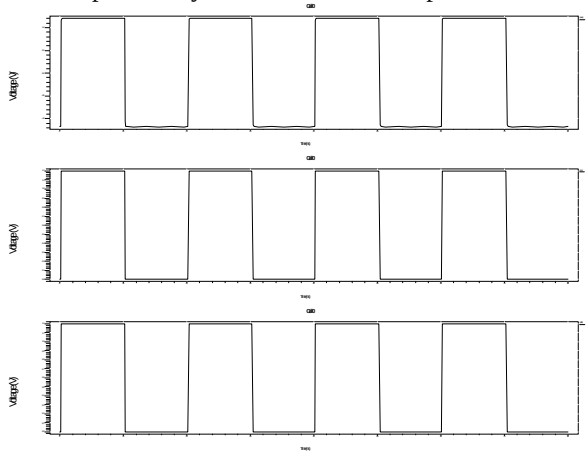

Fig.4. Waveform for domino logic

## IV. Removal of Charge Sharing Problem Using Weak PMOS Logic

One simple solution to eliminate charge sharing problem is just to add a weak PMOS pull-up device(with a small W/L ratio) to the dynamic CMOS stage output, which basically forces a high output level except there is a strong pull-down path amongst the output and the ground. It can be observed that the weak PMOS transistor will be turned on only when the precharge node voltage is retained high. Otherwise it will be turned off as output voltage becomes high.

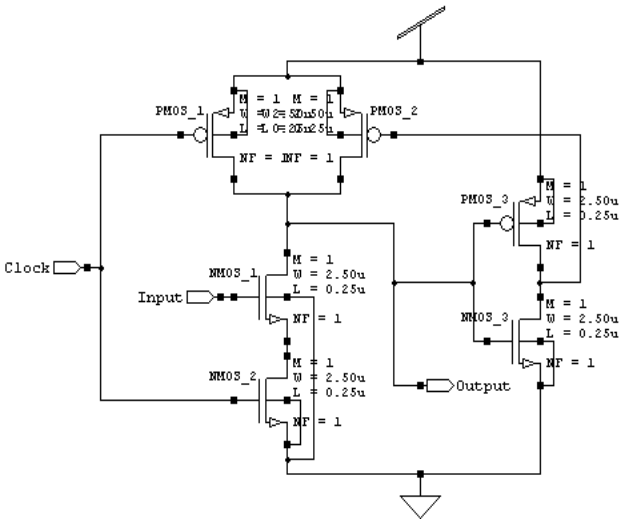


Fig.5. Weaker PMOS logic

Above we have implemented an inverter with weak PMOS by using simulation and generated its waveform. As we can see the waveform is sharp at both rising and falling edges and there is no charge sharing problem.

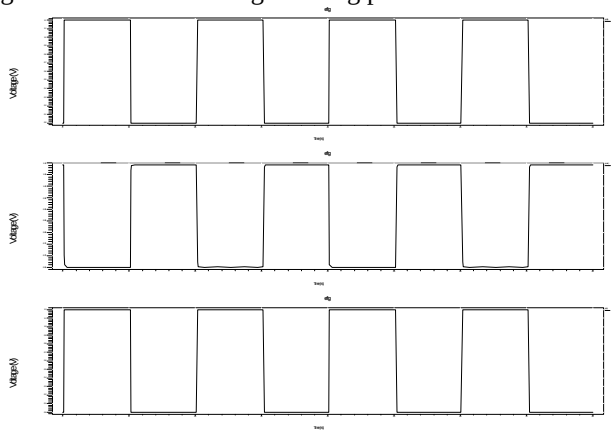

Fig.6. Waveform for weaker PMOS logic

## V. Results and Conclusions

In this paper we have studied the problem of charge sharing in dynamic logic circuits. Here we presented weak PMOS logic, whose purpose is to minimize the magnitude of the charge sharing problem, which is associated with the dynamic logic gate. The simulation results showed that weak PMOS logic offers an improvement in performance

of dynamic circuit under the same conditions. Hence the charge sharing problem in the dynamic circuit can be eliminate by adding a weak PMOS pull-up device to the dynamic CMOS stage output.

The table below shows the average power consumption in the different techniques using simulation.

Table 1: Power consumption in different technique

| Techniques | Average power consumed |
|---|---|
| Dynamic Logic | 1.423050e-004 watts |
| Domino Logic | 9.861521e-005 watts |
| Weak PMOS Logic | 3.662027e-004 watts |

## REFERENCES

[1] V. G. Oklobdziia and R. K. Montoye, "Design- performance trade-offs in CMOS domino logic," in Proc. IEEE Custom Integrated Circuits Conf., May 1985, pp. 334-337.

[2] J. A. Pretorius, A. S. Shubat, and C. A. T. Salama, "Charge redistribution and noise margins in domino CMOS Logic," IEEE Trans. Circuits Syst., vol. CAS-33,pp. 786-793, Aug. 1986.

[3] P. Larsson and C. Svensson, "Noise in digital dynamic CMOS circuits," IEEE J. Solid-State Circuits, vol. 29, pp. 655-662, June 1994.

[4] G. P. S'Souzw, "Dynamic logic circuit with reduced charge leakage," U.S. Patent 5 483 181, Jan. 1996.

[5] J. J. Coyino, "Dynamic CMOS circuits with noise immunity," U.S. Patent 5 650 733, July 1997.

[6] K. Roy, S. Mukhopadhyay, H.M. Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits". In proc., IEEE, vol. 91, no. 2, 2003, pp. 305-327.

[7] V. Kursun and E. G. Friedman, "Domino Logic with variable threshold voltage keeper, U.S. patent pending".

[8] Y.Ye, S. Borkar, andV. De, "A new technique for standby leakage reduction in high-performance circuits," in Proc. Symp. VLSI Circuits, 1998, pp. 40–41.

[9] V. Kursun and E. G. Friedman, "Domino logic with dynamic body biased keeper," in Proc. Eur. Solid-State Circuits Conf., Sept. 2002, pp.675–678.

[10] A. Alvandpour, P. Larsson-Edefors, and C. Svensson, "A leakage tolerant multi-phase keeper for wide domino circuits," in Proc. IEEE Int. Conf. Electronics Circuits Systems, Sept. 1999, pp. 209–212.

[11] A. Alvandpour, R. K. Krishnamurty, K. Soumyanath, and S. Y. Borkar,"A sub-130-nm conditional keeper technique," IEEE J. Solid-State Circuits, vol. 37, pp. 633–638, May 2002.

[12] G. Yang, Z.Wang, and S. Kang, "Leakage-proof domino circuit design for deep sub-100 nm technologies", Proc. IEEE Int. Conf. VLSI Des., 2004, pp. 222–227.

[13] Sung-Mo Kang and Yusuf Leblebici CMOS Digital Integrated Circuits – Analysis and Design, Tata McGraw Hill, 2003.

[14] M. W. Allam, M. H. Anis, and M. I. Elmasry, "High-Speed dynamic logic styles for scaled-down CMOS and MTCMOS technologies," in Proc. IEEE Int. Symp. Low-Power Electronics Design, July 2000, pp.155–160.

[15] V.Kursun and E.G. Friedman, "Domino logic with dynamic body biased keeper," Proc. IEEE Eur. Solid-State Circuits Conf., pp. 675–678, Sept. 2002.

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